# EXHIBIT 25

**IN THE UNITED STATES DISTRICT COURT**
**FOR THE WESTERN DISTRICT OF TEXAS**
**MIDLAND-ODESSA DIVISION**

| | | |
|---|---|---|
| **REDSTONE LOGICS LLC,** *Plaintiff,* | § | |
| **-v-** | § | **7:24-CV-00231-ADA** |
| **QUALCOMM INCORPORATED, QUALCOMM TECHNOLOGIES, INC.,** *Defendants.* | § | |

**CLAIM CONSTRUCTION ORDER AND MEMORANDUM IN SUPPORT THEREOF**

Before the Court are the Parties' claim construction briefs: Defendants Qualcomm Incorporated and Qualcomm Technologies, Inc.'s Opening and Reply briefs (ECF Nos. 27 and 29, respectively) and Plaintiff Redstone Logics LLC's Response and Sur-Reply briefs (ECF Nos. 28 and 30, respectively). The Court provided preliminary constructions for the disputed terms five days before the hearing. The Court held the *Markman* hearing on June 9, 2025. ECF No. 33. During that hearing, the Court informed the Parties of the final constructions for the disputed terms. *Id.* This Order does not alter any of those constructions.

## I. DESCRIPTION OF THE ASSERTED PATENTS

Plaintiff asserts U.S. Patent No. 8,549,339, which is entitled "Processor core communication in multi-core processor." The specification describes that the cores in prior art multi-core processors generally share the same supply voltage and clock signal. '339 Patent at 1:7–10. But to use dynamic voltage and frequency scaling—which is a technique that varies the

power supply voltage and clock frequency to reduce power consumption[1]—multiple supply voltages and multiple clock signals need to be provided to allow different cores to operate at different voltages and/or frequencies. *See id.*

The specification describes that the multi-core processor "may be further divided into regions." *Id.* at 2:20–21. Each region may have its own independent power profile that uses its own supply voltage and its own independent clock domain that has a phase lock loop ("PLL") to output its own clock signal. *Id.* at 2:26–31.

Claim 1 requires two sets of processor cores, each having their own supply voltage and their own clock signal.

> 1. A multi-core processor, comprising:
> a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;
> a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and
> an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

[1] The formula for switching power is $P = f * C_L * V_{DD}^2$, where f is the frequency of the clock signal, $C_L$ is the capacitance of the load (output), and $V_{DD}$ is the voltage of the supply voltage. As such, reducing the frequency linearly reduces the switching power while reducing the voltage of the supply voltage exponentially reduces the switching power.

## II. LEGAL STANDARD

### A. General principles

The general rule is that claim terms are generally given their plain-and-ordinary meaning. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*); *Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1347 (Fed. Cir. 2014), *vacated on other grounds*, 575 U.S. 959, 959 (2015) ("There is a heavy presumption that claim terms carry their accustomed meaning in the relevant community at the relevant time.") (internal quotation omitted). The plain-and-ordinary meaning of a term is the "meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips*, 415 F.3d at 1313.

The "only two exceptions to [the] general rule" that claim terms are construed according to their plain-and-ordinary meaning are when the patentee (1) acts as his/her own lexicographer or (2) disavows the full scope of the claim term either in the specification or during prosecution. *Thorner v. Sony Computer Ent. Am. LLC*, 669 F.3d 1362, 1365 (Fed. Cir. 2012). The Federal Circuit has counseled that "[t]he standards for finding lexicography and disavowal are exacting." *Hill-Rom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014). To act as his/her own lexicographer, the patentee must "clearly set forth a definition of the disputed claim term" and "'clearly express an intent' to [define] the term." *Thorner,* 669 F.3d at 1365.

"Like the specification, the prosecution history provides evidence of how the PTO and the inventor understood the patent." *Phillips*, 415 F.3d at 1317. "[D]istinguishing the claimed invention over the prior art, an applicant is indicating what a claim does not cover." *Spectrum Int'l, Inc. v. Sterilite Corp.*, 164 F.3d 1372, 1379 (Fed. Cir. 1998). The doctrine of prosecution disclaimer precludes a patentee from recapturing a specific meaning that was previously disclaimed during prosecution. *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1323 (Fed.

Cir. 2003). "[F]or prosecution disclaimer to attach, our precedent requires that the alleged disavowing actions or statements made during prosecution be both clear and unmistakable." *Id.* at 1325–26. Accordingly, when "an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable." *3M Innovative Props. Co. v. Tredegar Corp.*, 725 F.3d 1315, 1326 (Fed. Cir. 2013).

A construction of "plain and ordinary meaning" may be inadequate when a term has more than one "ordinary" meaning or when reliance on a term's "ordinary" meaning does not resolve the parties' dispute. *O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co*., 521 F.3d 1351, 1361 (Fed. Cir. 2008). In that case, the Court must describe what the plain-and-ordinary meaning is. *Id.*

"Although the specification may aid the court in interpreting the meaning of disputed claim language . . ., particular embodiments and examples appearing in the specification will not generally be read into the claims." *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1571 (Fed. Cir. 1988). "[I]t is improper to read limitations from a preferred embodiment described in the specification—even if it is the only embodiment—into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004).

Although extrinsic evidence can be useful, it is "less significant than the intrinsic record in determining 'the legally operative meaning of claim language.'" *Phillips*, 415 F.3d at 1317 (quoting *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004)). Technical dictionaries may be helpful, but they may also provide definitions that are too broad or not indicative of how the term is used in the patent. *Id.* at 1318. Expert testimony may also be helpful, but an expert's conclusory or unsupported assertions as to the meaning of a term are not. *Id.*

**B. Claim differentiation**

Under the doctrine of claim differentiation, a court presumes that each claim in a patent has a different scope. *Phillips*, 415 F.3d at 1314–15. The presumption is rebutted when, for example, the "construction of an independent claim leads to a clear conclusion inconsistent with a dependent claim." *Id.* The presumption is also rebutted when there is a "contrary construction dictated by the written description or prosecution history." *Seachange Int'l., Inc. v. C-COR, Inc.*, 413 F.3d 1361, 1369 (Fed. Cir. 2005). The presumption does not apply if it serves to broaden the claims beyond their meaning in light of the specification. *Intellectual Ventures I LLC v. Motorola Mobility LLC*, 870 F.3d 1320, 1326 (Fed. Cir. 2017).

**C. Indefiniteness**

"[I]ndefiniteness is a question of law and in effect part of claim construction." *ePlus, Inc. v. Lawson Software, Inc.*, 700 F.3d 509, 517 (Fed. Cir. 2012). Patent claims must particularly point out and distinctly claim the subject matter regarded as the invention. 35 U.S.C. § 112, ¶ 2. A claim, when viewed in light of the intrinsic evidence, must "inform those skilled in the art about the scope of the invention with reasonable certainty." *Nautilus Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 910 (2014). If it does not, the claim fails § 112, ¶ 2 and is therefore invalid as indefinite. *Id.* at 901. Whether a claim is indefinite is determined from the perspective of one of ordinary skill in the art as of the time the application was filed. *Id.* at 911.

## III. LEGAL ANALYSIS

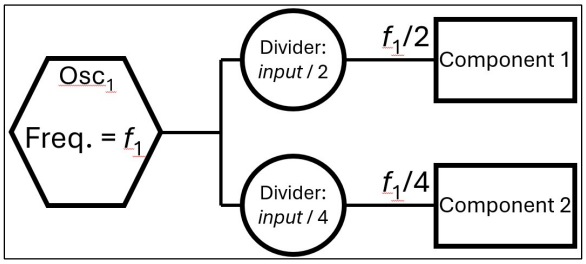
### A. Term #1: "the first clock signal is independent from the second clock signal"

| Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| #1: "the first clock signal is independent from the second clock signal"<br><br>U.S. Patent No. 8,549,339, Claims 1, 21<br><br>Proposed by Defendants | Plain and ordinary meaning | Plain and ordinary, which requires that the first and second clock signals depend from different reference oscillator clocks |

**The Parties' Positions:**

The parties dispute whether the first and second clock signals must come from different oscillators to be independent (Defendants' position) or whether they can come from the same oscillator, *i.e.*, a single oscillator (Plaintiff's position). Opening at 5, Response at 2.

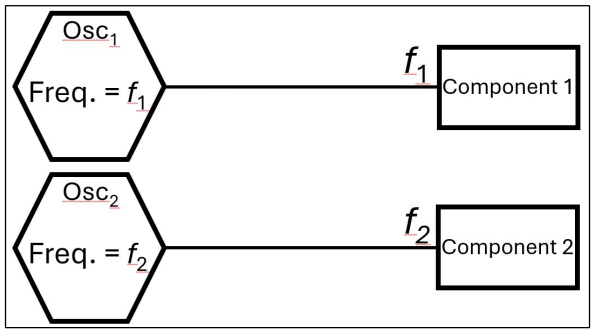
Defendants first contend that the plain meaning of "independent" cannot only mean "different." Opening at 5. Defendants contend that the example below depicts a single reference oscillator that is the source for two clock signals.




*Id.* at 6. Defendants contend that "[a] ***single reference oscillator approach*** may provide multiple different clocks derived from—and ***dependent on***—the same reference oscillator source." *Id.* (citing Opening, Ex. 1 (Villasenor Decl.) at ¶ 44) (emphases in Defendants' brief). Defendants contend that "[c]lock signals at $f_1/2$ and $f_1/4$ ***do not*** meet the plain and ordinary meaning of

'independent' because they remain dependent on the same input, namely clock frequency $f_1$ provided by reference oscillator $Osc_1$." *Id.* (citing Opening, Ex. 1 (Villasenor Decl.) at ¶ 44) (emphasis in Defendants' brief). Defendants contend that this example "demonstrates that two clock signals, such as $f_1/2$ and $f_1/4$, may be different but not independent[.]" *Id.*

Defendants contend that, in contrast with the above figure, using separate oscillators results in "multiple clock signals that are ***not dependent*** on the same reference oscillator[.]" *Id.* at 8 (emphasis in Defendants' brief).




Defendants contend that "when separate reference oscillators are used, the resulting clock signals are independent." *Id.*

Defendants contend that Plaintiff, in a prior case, argued that if the scaling factors for the frequency dividers for the two clock signals were independent from each other, then the two clock signals (*i.e.*, the output of the frequency dividers) would likewise be independent. *Id.* at 7. But Defendants contend that "[e]ven if two or more factors may affect the frequency of the resulting clock signals, that fails to negate the fact that each of these clock signals remains dependent upon the same reference oscillator." *Id.* (citing Opening, Ex. 1 (Villasenor Decl.) at ¶ 45). Defendants contend that Plaintiff's argument is incorrect because "it ignores the necessary dependence that exist on the single reference oscillator." *Id.* at 8.

Defendants contend that the prosecution history also confirms that while two clock signals derived from a single reference oscillator clock may be "different," they are not "independent."

*Id.* More specifically, Defendants contend that because Applicant distinguished the single oscillator approach in the Kim prior art reference, this demonstrates that "[t]he intrinsic record statements confirm that the plain and ordinary meaning of the Independent Term requires 'different reference oscillator clocks.'" *Id.* at 9. Defendants contend that Kim discloses a single reference oscillator (clock source 270) "that feeds a 'main PLL 260,' which includes 'one ***or more frequency dividers***' to generate multiple ***different*** clock signals[.]"

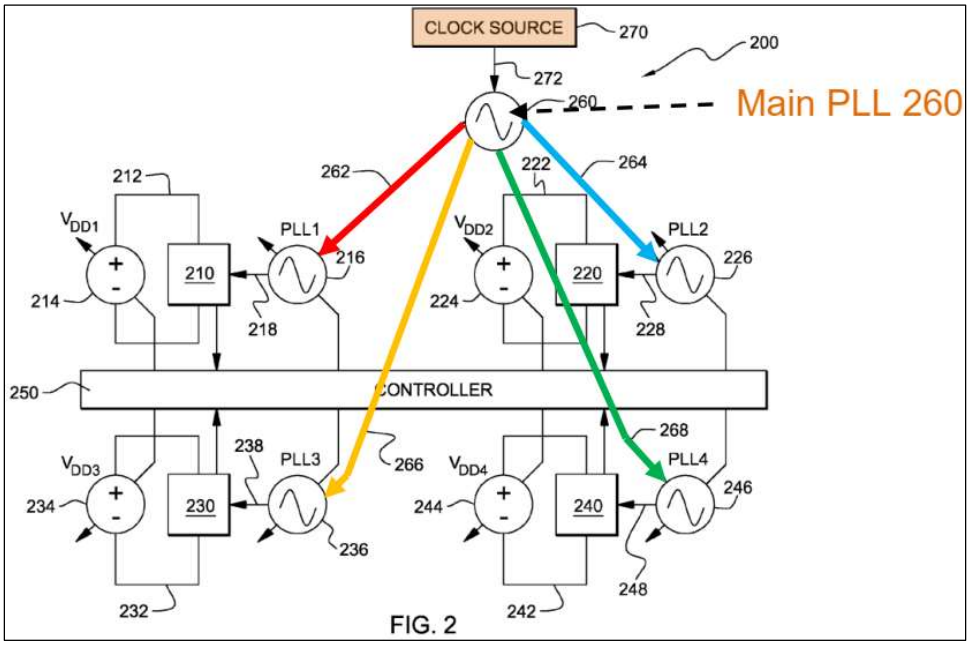


FIG. 2

*Id.* (emphases in Defendants' brief, alterations to Figure 2 added by Defendants). Defendants contend that "[a] change to the frequency of clock source 270 will impact each of clock signals 262, 264, 266, and 268, such that they are not independent of each other." *Id.* at 10. Defendants contend that, during prosecution, Applicant made the following argument:

**File History – Response to Office Action 8/29/2012**

In addition, *Kim* also fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal, respectively. In addition, the first clock signal is independent from the second clock signal. Instead, *Kim* discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having a single clock source (i.e., 170 in FIG. 1 or 270 in FIG. 2). The clock signal from this single clock source is then processed (i.e., divided or multiplied) and provided to each of the cores. See *Kim*, paragraphs [0024]-[0025] and FIGs 1 – 2.

*Id.* (citing Opening, Ex. H at 10–11 (alternations added by Defendants)). Defendants contend that the highlighted portion "makes clear applicants' position: Despite Kim's[2] Figure 2 disclosing clock signals 262 and 264 that are ***different*** based on separate dividers in main PLL 260, that is not good enough to meet the 'independent' language because they originate from 'a single clock source,' namely clock source '270.'" *Id.* (emphasis in Defendants' brief). Defendants contend that "[b]y reciting the 'independent' language and distinguishing that language ('[i]nstead') from Kim's disclosure of multiple different clock signals fed by a 'single clock source,' the applicant expressly disclaimed a construction of the Independent Term that would encompass two different signals processed from a single clock source, *i.e.*, an oscillator." *Id.* (alteration in Defendants' brief).

Defendants contend that, to the extent that Plaintiff will argue that Applicant distinguished Kim on other grounds, including because Kim does not disclose "sets" of processor cores, Federal Circuit law does not limit the scope of surrender to what was required to avoid prior art, rather, applicants can surrender more than necessary. *Id.* at 11 (citing cases).

Even if Applicant's statements do not rise to the level of a disclaimer, Defendants contend that they still inform the plain-and-ordinary meaning of this term. *Id.* In particular, Defendants contend that Applicant "used 'independent' repeatedly both throughout the response and specific

[2] The Court has unitalicized all instances of "Kim" and "Jacobwitz" in the parties briefs in order to have the same formatting throughout this order.

to Kim in explaining why the examiner's art was insufficient" and "separately argued that Kim and its multiple different clocks feeding different PLLs was distinguishable because it employed a single clock source." *Id.* (citing Opening, Ex. H at 11). Defendants contend that Applicant distinguished Kim based on that the clock signals were "independent" and not merely "different." *Id.*

In its response, Plaintiff contends that Defendants' proposed construction improperly requires that the first and second clock signals cannot depend on a third signal (*i.e.*, the output of the oscillator) where there is no support for that in the claim language, intrinsic record, or prior art. Response at 2. Plaintiff contends that it does not assert that "'independent' should be construed to mean 'different,' rather, [Plaintiff] observes that 'different' is the only clarification on the plain meaning of 'independent' actually supported by the intrinsic record." *Id.*at 3 n.3.

Plaintiff contends that the prosecution history demonstrates that the first and second clock signals do not need to come from different reference oscillator clocks to be "independent." *Id.* at 3. More specifically, Plaintiff contends that Examiner rejected the independent claims as anticipated by the Jacobowitz prior art reference. *Id.* (citing Opening, Ex. F at 4–5). Plaintiff contends that "Applicant amended the independent claims to distinguish the input and output of the PLLs and specify that the inputs of the two PLLs must be independent[.]" *Id.* at 3. Plaintiff contends that Applicant then argued that "Jacobowitz merely distributes a single signal, $V_R$, to the local oscillators" and thus does not disclose "a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal as input" or that "the first clock signal is independent from the second clock signal." *Id.* at 4 (citing Opening, Ex. H at 10–11).

With respect to the Kim prior art reference, Plaintiff contends that Applicant argued that Kim disclosed a "multi-core processor … having a single clock source … [that] is then processed … and ***provided to each of the cores***" and thus "does not disclose any of the claimed clock signals or that the first and second clock signals are independent." *Id.* at 4–5 (citing Opening, Ex. H at 10–11) (emphasis in Plaintiff's brief). Plaintiff contends that Applicant also argued that Jacobowitz and Kim do not disclose "***sets of processor cores*** configured to receive multiple and independent clock signals." *Id.* at 5 (citing Opening, Ex. H at 10–11) (emphasis in Plaintiff's brief). Plaintiff contends that "[b]ecause there are no sets of processor cores, there are no first and second supply voltages that they are configured to dynamically receive." *Id.* Plaintiff contends that the same is true for the "first and second output clock signals," namely, because there are no clock signals in Jacobowitz and Kim that input to the "sets of processor cores," then "these signals do not exist to be independent." *Id.* Plaintiff contends that "[e]ach and every time the Applicant discussed 'independent,' it was to explain it is not met because the core architecture is wrong and thus no arrangement of clock signals could meet the limitations." *Id.* at 6.

With respect to Defendants' argument that "applicant expressly disclaimed a construction of the Independent Term that would encompass two different signals processed from a single clock source[,]" Plaintiff contends that "Applicant clearly made the argument that without sets of cores, there can be none of the claimed signals, including the clock signals." *Id.* at 5–6. Plaintiff contends that the fact Applicant made this argument three times, Defendants cannot overcome the "heavy presumption against disclaimer." *Id.*

Plaintiff contends that "there is no explanation or support for this notion that signals derived from a common source cannot be independent from one another" and that Defendants' expert "does not, and presumably cannot, show any evidence that POSITAs at the time considered

a common 'mathematical[] deriv[ation]' of two signals to be a dependence of one of those signals on the other." *Id.* at 7 (alterations in Plaintiff's brief). Plaintiff contends that Defendants' expert's opinion is "entirely conclusory and thus not useful." *Id.* (citing *Phillips*, 415 F.3d at 1218–19).

With respect to Defendants' single clock oscillator example, Plaintiff contends that the two clock signals are independent because the divisors of the PLLs are independently variable. *Id.* at 17–8.

In their reply, Defendants contend that while Plaintiff asserts that it, in this case, is not arguing "independent" should be construed as "different," Plaintiff previously argued that "[i]f the Court finds that 'independent' needs clarification—it does not—it merely means 'different'" and "'independent' is best understood as simply meaning 'different.'" Reply at 1 (citing Opening, Ex. 2 at 7, 2). Defendants contend that Plaintiff's shifting arguments indicates that this term should be construed. *Id.*

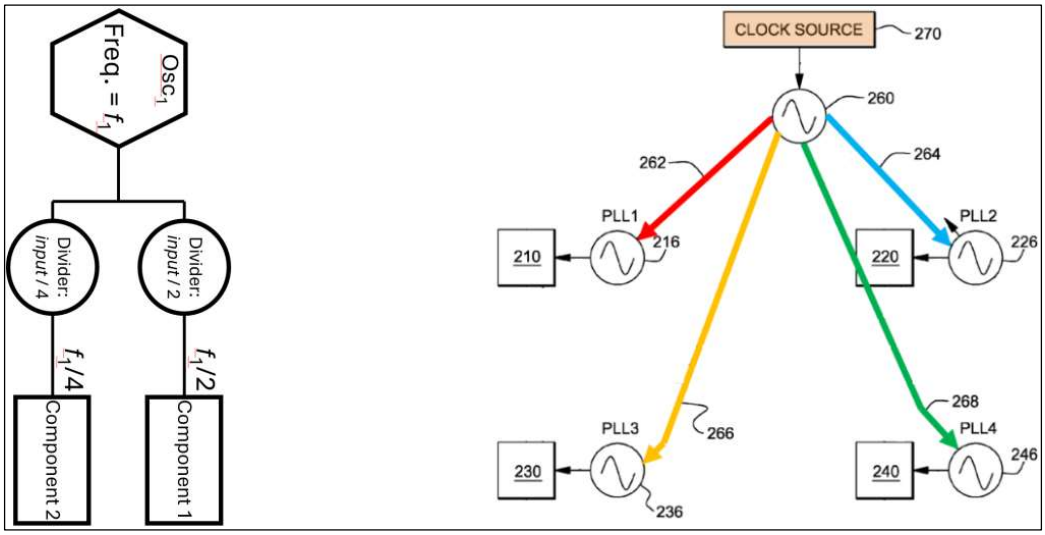
Defendants contend that Applicant disclaimed "mere different signals" during prosecution. *Id.* More specifically, Defendants contend that Applicant argued that a single clock source split into multiple signals in Kim did not meet the "independent" requirement. *Id.* at 2 (citing Opening, Ex. H at 10–11).

With respect to Plaintiff's "third signal" argument, Defendants contend that "Applicant itself chose to amend its claims to include 'independent' clocks, and [Defendants] correctly point out that two clocks derived from the same source are not independent." *Id.*

Defendants contend that Plaintiff's arguments regarding the Jacobowitz prior art reference are irrelevant to Applicant's argument regarding the Kim prior art reference. *Id.* at 2–3. Furthermore, Defendants contend that the prosecution history does not support Plaintiff's assertions regarding the Applicant's arguments for Jacobwitz. *Id.* at 3.

Defendants contend that Plaintiff's argument regarding Applicant distinguishing Kim based on a lack of sets of processor cores and independent voltages only serves to provide additional grounds to distinguish prior art, but does not otherwise rebut a prosecution disclaimer regarding whether "the first clock signal is independent from the second clock signal." *Id.* Defendants also contend that "whether Kim discloses sets of cores is immaterial to the Applicant's argument that Kim's 'single clock source' arrangement does not satisfy the claims' independent clock requirement." *Id.* (citing Opening at 9–10).

Defendants contend that their example with a single clock source is similar to Figure 2 in Kim in that (1) both figures have a single clock source ($O_{SC1}$ and clock source 270, respectively) and (2) the resulting clock signals in both figures are inputs to components 1 and 2, and cores 210, 220, 230, and 240, respectively.




*Id.* at 4–5 (rotation of left figure and annotations to right figure in Defendants' brief).

Defendants contend that "[t]he plain and ordinary meaning of 'independent' requires more than merely 'different' signals." *Id.* at 5.

In its sur-reply, Plaintiff contends that Defendants make the same "faulty arguments" that the Court already rejected in a prior case. Sur-Reply at 1.

Plaintiff contends that Defendants' proposed construction "has no support beyond the arguments [they] wish[] the applicant had made in prosecution." *Id.* Plaintiff contends that Defendants' proposed construction improperly focuses on a "third signal"—the output of the clock oscillator—which is not mentioned in the claims. *Id.*

Plaintiff contends that Defendants' "creative interpretation of the file history around Kim hardly amounts to anything 'unequivocal[]' as it claims." *Id.* Rather, Plaintiff contends that "applicant identified two limitations Kim failed to disclose and explains instead of meeting *both* sets of limitations, Kim disclosed an apparatus providing clock signals to each of the cores[.]" *Id.* at 1–2 (emphasis in Plaintiff's brief).

Plaintiff contends that if the focus of "'independent' was on the origin of the clock signals, the applicant would have argued that distinction as to both Jacobowitz and Kim." *Id.* at 2. Plaintiff contends that despite the fact that Jacobowitz discloses a single clock source, "Applicant never made even a colorable argument that Jacobowitz failed to disclose 'independent' clock signals because of the singular source." *Id.*

In addition, Plaintiff contends that Applicant focused on "independent" when distinguishing Kim based on a lack of sets of processor cores and that "[t]his is the only consistent use of 'independent': where there are no sets of processor cores, there are not claimed independent clock signals or voltages." *Id.* at 3 (citing Opening, Ex. H at 10, 10–11).

With respect to Defendants' argument that any two frequency functions that include a common variable cannot be independent, Plaintiff contends that Defendants have "not shown a POSITA has ever considered "independence" of two signals relies on an upstream signal." *Id.* at 3, 4. Plaintiff contends that the only non-conclusory testimony provided by Defendants' expert "would render any two signals on a single device not independent." *Id.* at 4 (citing Response at 8).

Plaintiff further contends that Defendants have not shown that Applicant or Examiner took that position. *Id.*at 5.

**The Court's Analysis:**

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Plaintiff that this term should be construed according to its plain-and-ordinary meaning for the reasons that follow. ***First***, the "heavy presumption" is that terms should be construed according to their plain-and-ordinary meaning. *Azure Networks*, 771 F.3d at 1347.

***Second***, the Court disagrees with Defendants that the plain meaning of "independent" requires that the first and second clock signals must use separate clock oscillators. The claim term focuses on the relationship between the first and second clock signals, and not the relationships between the first clock signal and its clock oscillator, and second clock signal and its clock oscillator. Furthermore, the claims do not even mention or require a "clock oscillator," let alone in any particular arrangement with respect to the first and second clock signals. Furthermore, the word "oscillator" does not even appear in the specification.

***Third***, the only two exceptions to the general rule that a term should be construed as having its plain-and-ordinary meaning are lexicography and disclaimer. *Thorner*, 669 F.3d at 1365. Defendants do not allege lexicography, but do allege that Applicant disclaimed the use of a single clock oscillator while distinguishing the Kim prior art reference during prosecution. While it is somewhat of a close call, the Court concludes that Applicant did not disclaim use of a clock oscillator that is shared by the first and second clock signals.

The first reason why the Court concludes there is no disclaimer is because Kim does not disclose first and second clock signals. More specifically, the claim language describes that the

first and second ***sets*** of processor cores of the multi-core processor receive the first and second clock signals, respectively. '339 Patent, Claim 1, Limitation [a]; Claim 1, Limitation [c]; Claim 21, Limitation [a]; Claim 21, Limitation [c]. Applicant argued that Kim does not disclose ***sets*** of cores, but rather single cores. Opening, Ex. H at 10 ("Instead, Kim discloses having each core, not a set of processor cores, received a $V_{DD}$"). Applicant distinguished Kim based on this requirement. *Id.* at 11 ("The clock signal from this single clock source is then processed (i.e., divided or multiplied) and provided to each of the cores."); 11 ("As discussed above, neither Jacobowitz nor Kim discloses having sets of processor cores configured to receive multiple and independent clock signals."). Because the clock signals in Kim are provided to individual cores, and not sets of cores, the clock signals in Kim are not the first and second clock signals of Claims 1 and 21, which must be provided to sets of cores. Concomitantly, because the clock signals in Kim are not the first and second clock signals, they likewise cannot meet the requirement that "the first clock signal is independent from the second clock signal." Because Applicant's prosecution statements were directed at differentiating Kim based on its failure to disclose sets of cores and, concomitantly, first and second clock signals that are received by those sets of cores, the Court concludes that there was no disclaimer. *3M Innovative Props.*, 725 F.3d at 1326 (when "an applicant's statements are amenable to multiple reasonable interpretations, they cannot be deemed clear and unmistakable.").

To the extent that Defendants were to argue that this is a hyper technical distinction, the Court disagrees. For disclaimer to attach, an applicant's statement must be clear and unmistakable. *Genuine Enabling Tech. LLC v. Nintendo Co.*, 29 F.4th 1365, 1374 (Fed. Cir. 2022). Furthermore, "[t]he standards for finding lexicography and disavowal are exacting." *Hill-Rom Servs.*, 755 F.3d at 1371. As such, even if this were the only reason against disclaimer, the Court concludes that

Defendants have not met the high standard to show that Applicant disclaimed single clock oscillators.

The second reason why the Court concludes there is no disclaimer is because it appears Applicant may have understood Kim to disclose that PLL1, PLL2, PLL3, and PLL4 could not be independently varied, but were all set to same value by controller 250. More specifically, Applicant argued that "[t]he clock signal from this single clock source is then processed (i.e., divided or multiplied) and provided to each of the cores." Opening, Ex. H at 11. This statement does not disclose that the clock signal from the single clock source is ***independently*** divided or multiplied by a different amount by each of the four PLLs. Rather, this statement appears to indicate that each PLL either divides or multiplies the clock signal from the single clock source by the same amount, *i.e.*, the frequency scaling of the PLLs are not independent. As such, to the extent Kim disclosed a first and second clock signal, Applicant may have distinguished Kim based on the fact that the first clock signal is not independent from the second clock signal because they cannot be varied independently and thus are effectively the same signal. Obviously, if the first clock signal is the exact same signal as the second clock signal, the first clock signal is not independent from the second clock signal.

The paragraphs that Applicant cites from Kim ([0024] and [0025]) support this interpretation. Paragraph [0024] is the corresponding description of Figure 1, which does not depict multiple PLLs. Paragraph [0025] is the corresponding description of Figure 2, which does have multiple PLLs.

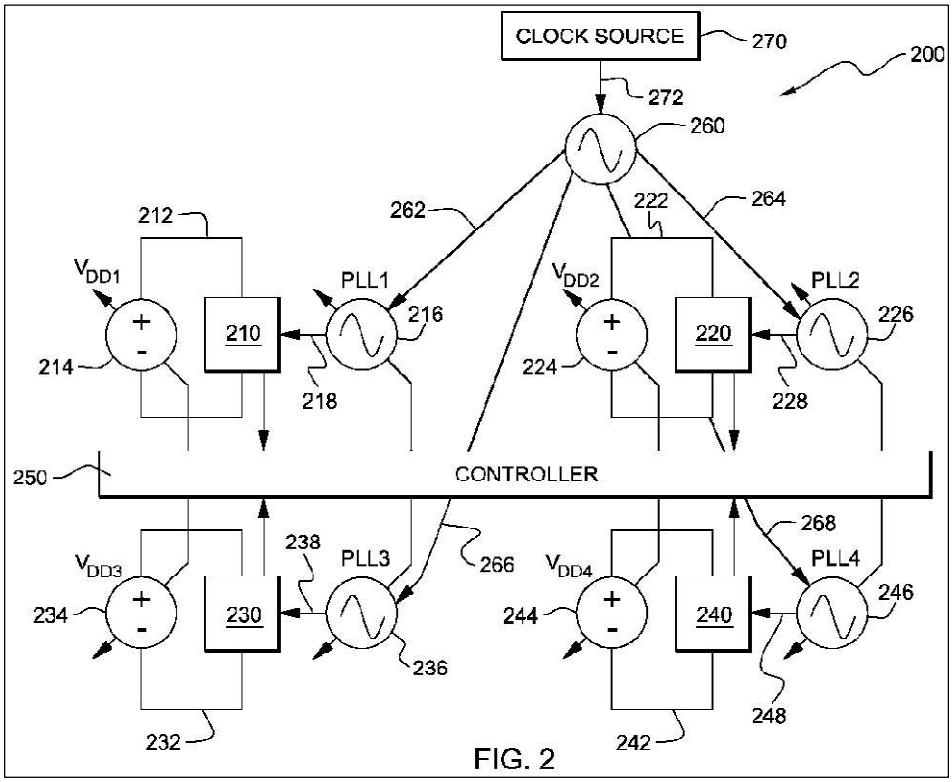



FIG. 2

Paragraph [0025] describes that PLL1 216, PLL2 226, PLL 236, and PPL 246 "further multiply the output clock frequency received from the main PLL 260 in order to deliver a reference input clock frequency that is higher than the input clock frequency received from the main PLL 260." U.S. Patent Application 2009/0138737 (Kim) at [0025]. This paragraph further explains that PLL 260 outputs a clock frequency that is a "first multiple of the clock frequency provided by the clock source 270." *Id.* This paragraph continues

> Further, each of the PLLs, PLL1 (reference numeral 216), PLL2 (reference numeral 226), PLL3 (reference numeral 236) and PLL4 (reference numeral 246), delivers a reference input clock frequency (indicated by arrows 218, 228, 238 and 248) that is a further multiple of the clock frequency provided (arrow 272) by the clock source 270."

*Id.* Notably, nothing in paragraph [0025] expressly describes that each of the clock frequencies of PLL1 216, PLL2 226, PLL 236, and PPL 246 are different or that the multipliers are different. Rather, this paragraph describes that PLL1 216, PLL2 226, PLL 236, and PPL 246 only "further

multiply" the frequency of the clock signal from PLL 260. Had Kim intended to disclose that PLL1 216, PLL2 226, PLL 236, and PPL 246 in Figure 2 could scale the frequency independently, Kim could have easily written that "each of the PLLs … delivers a reference input clock frequency … that ***are*** further multiple***s*** of the clock frequency provided (arrow 272) by the clock source 270." As such, Applicant may have understood Kim to disclose that PLL1 216, PLL2 226, PLL 236, and PPL 246 could not be independently varied and distinguished the claimed invention accordingly.

The third reason is that while Jacobwitz, like Kim, disclosed using a single clock oscillator, Applicant did not distinguish Jacobowitz for having a single clock source like Applicant did for Kim. Opening, Ex. H at 9–11. This further indicates that Applicant's prosecution statements for Kim did not disclaim using a single clock oscillator.

Therefore, for the reasons stated above, the Court concludes that Defendants have met "exacting" requirements for a "clear and unmistakable" disclaimer. *Hill-Rom Servs.*, 755 F.3d at 1371; *Genuine Enabling Tech. LLC*, 29 F.4th at 1374.

Therefore, for the reasons described above, the Court finds that the term should be construed according to its plain-and-ordinary meaning, wherein the plain and ordinary meaning does not require that the first and second clock signals depend from different reference oscillator clocks.

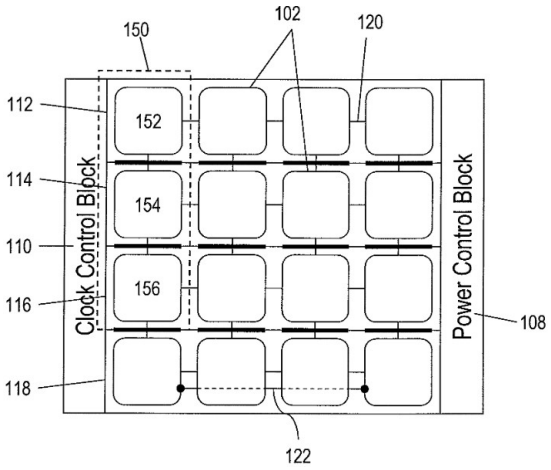
**B. Term #2: "located in a periphery of the multi-core processor"**

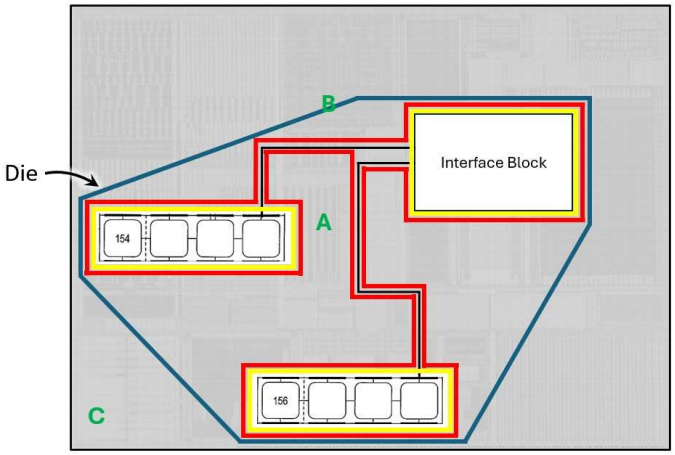
| Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| #2: "located in a periphery of the multi-core processor"<br><br>U.S. Patent No. 8,549,339, Claim 5<br><br>Proposed by Defendants | Plain and ordinary meaning | Indefinite |

**The Parties' Positions:**

Defendants contend that this claim term is ambiguous because "claim 5's use of the vague term 'periphery' coupled with the lack of any required physical relationship between the components of the multicore processor, which may be spaced apart from each other." Opening at 13.

Defendants contend that to determine whether the control block(s) are "located in the periphery of the multicore processor," the first step is to identify the location of the processor cores. *Id.* Defendants contend that while the patent presents a simple grid arrangement of processor cores (below left), the placement of real world processors on a die may be in a non-grid arrangement (below right).




*Id.* at 14–15 (citing '339 Patent at Figure 1; Opening, Ex. 1 (Villasenor Decl.) at Figure G, ¶ 69). Defendants contend that the figure to the right depicts potential "peripheries" in yellow, red, and blue while locations A, B, and C indicate where a control block may be placed. *Id.* at 15. Defendants contend that a POSITA cannot know with reasonable certainty which location is the claimed "periphery" and "the language of claim 5 provides no guidance[.]" *Id.* (citing Opening, Ex. 1 (Villasenor Decl.) at ¶¶ 62, 72, 68).

Defendants contend that specification also does not provide any guidance. *Id.* In particular, Defendants contend that "periphery" only appears once in the specification, and even then it "merely parrots claim 5 and offers no additional guidance[.]" *Id.* at 16 (citing Opening, Ex. 1 (Villasenor Decl.) at ¶ 72).

Defendants contend that while a POSITA may be able to determine with reasonable certainty where the "periphery" is in Figure 1, this does not render this claim term to be not indefinite in non-grid layouts. *Id.*

In its response, Plaintiff contends that "periphery" has "a plain, geometric, meaning" to a POSITA and the scope of "a periphery of the multi-core processor" is "clear from the intrinsic evidence." Response at 8–9.

Plaintiff contends that the specification describes that "the power control block 108 and the clock control block 110 may be arranged at two different sides of the multi-core processor 100 as shown in FIG. 1." *Id.* at 9 (citing '339 Patent at 2:34–36). Based on that, Plaintiff contends that the specification "thus clarifies the metes and bounds of the multi-core processor, placing the control blocks at its edge or periphery of the Figure 1 example." *Id.* Plaintiff contends that there is "no ambiguity in either term and no need to consider extrinsic evidence." *Id.*

With respect to Defendants' examples, Plaintiff first contends that it "agrees many different arrangements of sets of cores may exist, but they are still bound to a rational and useful arrangement." *Id.* at 10. Plaintiff contends that Defendants' examples lack important detail that a POSITA would expect in a multi-core processor. *Id.* With respect to the above example with locations A, B, and C, Plaintiff also contends that "there is no support for the notion that such an arrangement would exist or would be considered by a POSITA when contemplating the scope of

'periphery[,]'" and Defendants only cite their expert's conclusory declaration to support such an arrangement. *Id.* (citing Opening at 15).

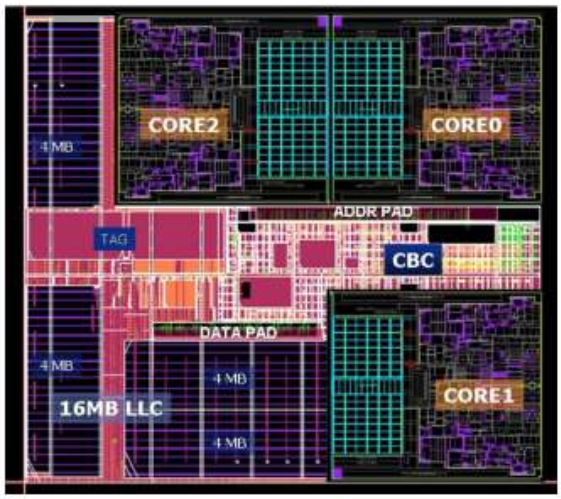
Plaintiff contends that Defendants do not argue that "periphery" and/or "multi-core processor" are inherently indefinite and, as such, Defendants do not provide any arguments outside their examples. *Id.* at 12.

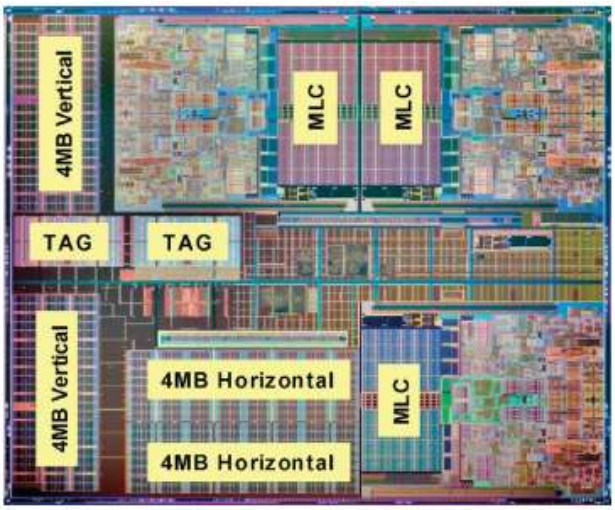
In their reply, Defendants contend that Plaintiff "relies heavily" on the simplistic example of Figure 1. Reply at 6.

With respect to Defendants' examples, Defendants contend that Plaintiff does not substantively address those examples, but rather "attempts to undercut the illustrative architectures and expert testimony that highlight this term's indefiniteness." *Id.* Defendants contend that the "supposedly missing power and frequency inputs are provided by the very control blocks that Claim 5 requires be 'located in a periphery of the multi-core processor'—*i.e.*, the components that cannot be placed due to this term's indefiniteness." *Id.* at 7.

Defendants contend that their expert is a POSITA and opined that he considered the arrangements depicted in Defendants' examples and provided evidence that a POSITA would also do so. *Id.* (citing Opening, Ex. 1 (Villasenor Decl.) at ¶¶ 69, 70). Defendants contend that *Phillips* "endorses the very 'purposes' for which Dr. Villasenor's explanation is offered," *e.g.*, explaining the background of the technology, help the court understand what a POSITA would understand the claim term to mean, *etc.* *Id.* Defendants contend that, by contrast, Plaintiff did not provide an expert declaration, but rather "provides unsupported attorney argument masquerading as expert opinion for this term in at least five places." *Id.* (citing Response at 8, 10).

Defendants contend that their examples are "not 'unusual'," as there are "many distributed architectures existed in the industry prior to and at the time of the '339 Patent, including in Intel products such as the depicted Dunnington processor[.]"




*Id.* at 8 (citing Reply, Ex. 6 at Figures 2, 3). Defendants contend that "[i]n real-world configurations with sets of processor cores and an interface block spaced apart on the chip, a POSITA could not understand with reasonable certainty what constitutes the 'periphery' of such a multi-core processor." *Id.*

In its sur-reply, Plaintiff contends that Defendants effectively concede that the intrinsic record demonstrates no ambiguity or indefiniteness. Sur-Reply at 5. Plaintiff further contends that Defendants do not allege that the meaning of "periphery" or "multi-core processor" are ambiguous based on the intrinsic record. *Id.* Plaintiff contends that while Defendants assert that Figure 1 is "simple and idealized," they do not demonstrate an ambiguity in the intrinsic record, but rather improperly focus on extrinsic evidence provided by their expert. *Id.* at 5–6 (citing cases).

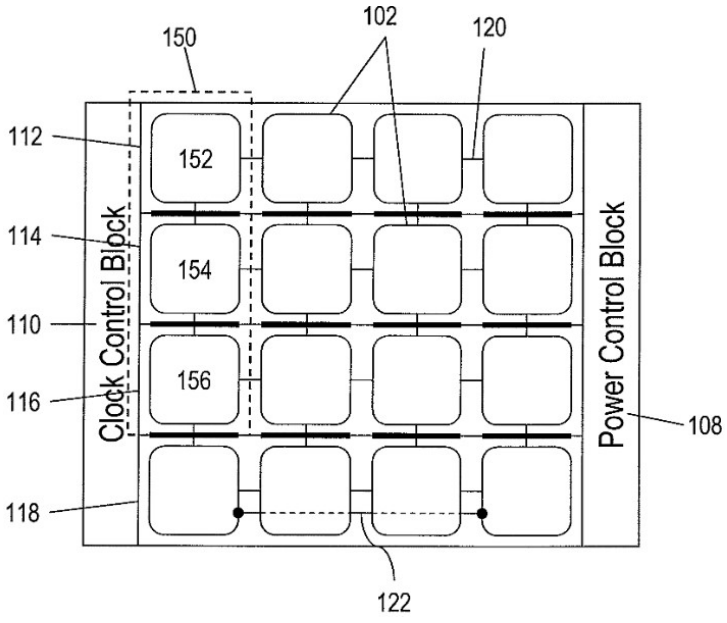
Plaintiff contends that "Instead of showing what a POSITA might be faced with and explaining the confusion it would cause, [Defendants' expert] shuffles blocks around with no regard for what a functioning processor might require." *Id.* at 6. With respect to Defendants'

argument based on the Intel Dunnington processor, Plaintiff contends that this exhibit demonstrates that the layout of processor cores is not as simple as Defendants argue and that the layout was a "compact and logical arrangement, not sets of cores placed well away from each other with no supporting infrastructure." *Id.* at 7. More specifically, Plaintiff contends that, in the Dunnington multi-core processor, the sets of cores are tightly bundled with the associated Mid-Level Caches, and the Last Level Cache and the Caching Bridge Controller are directly adjacent to the core-pairs. *Id.* (citing Reply, Ex. 6 at 230).

**The Court's Analysis:**

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Plaintiff that the term is not indefinite for the reasons that follow. ***First***, the term "periphery" is a plain English word with a non-technical meaning and Defendants do not allege that this word is ambiguous. Similarly, Defendants do not allege that "multi-core processor" is ambiguous.

***Second***, the parties agree that there is there is no ambiguity in the intrinsic evidence. Figure 1 provides depicts how control blocks are at the periphery of the set of processor cores.



While Defendants contend that this example is "simplified," the location of the clock and power control blocks is consistent with the plain meaning of "periphery."

***Third***, many of Defendants' arguments are based on extrinsic evidence, *e.g.*, Opening, Ex. 1 (Villasenor Decl.) at Figure G and Reply, Ex. 6 at Figure 2, which is improper for the Court to rely on when there is no ambiguity in the intrinsic record. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1583 (Fed. Cir. 1996) ("In those cases where the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper.").

***Fourth***, even if the Court were to consider Defendants' extrinsic evidence, the Court would not conclude that term is indefinite. The Court agrees with Plaintiff that the hypothetical examples that Defendants use in their Opening brief lack important detail and do not represent how cores in a multi-core processor are actually arranged across a die.

With respect to the Dunnington processor, the Court agrees with Plaintiff that the layout is "compact and logical," and where the cores are placed next to the Mid-Level Caches and close to the Last Level Cache in order to reduce the apparent memory latency, or possibly to improve bandwidth by allowing for shorter, but wider memory busses. Similarly, the Caching Bridge Controller is placed near the Mid-Level Caches (also in order to reduce the apparent memory latency), which is also near the cores. Furthermore, the cores and Mid-Level Caches are arranged in a grid pattern, which would be even more apparent if there were four pairs of dual cores. The Court concludes that, given the logic of where the cores are located and design constraints, a POSITA would be able to determine, with at least reasonable certainty, the "periphery of the multi-core processor." *Nautilus*, 572 U.S. at 910.

For these reasons, the Court concludes that Defendants have not provided clear and convincing evidence that this term is indefinite.

***Construction***: Because the "heavy presumption" is that terms should be construed according to their plain-and-ordinary meaning and because Defendants does not allege lexicography or disclaimer, which are the only two exceptions to the general rule that a term should be construed as having its plain-and-ordinary meaning, the Court concludes that the term should be construed as having its plain-and-ordinary meaning. *Azure Networks*, 771 F.3d at 1347; *Thorner*, 669 F.3d at 1365.

Therefore, for the reasons described above, the Court finds that the term is not indefinite and should be construed according to its plain-and-ordinary meaning.

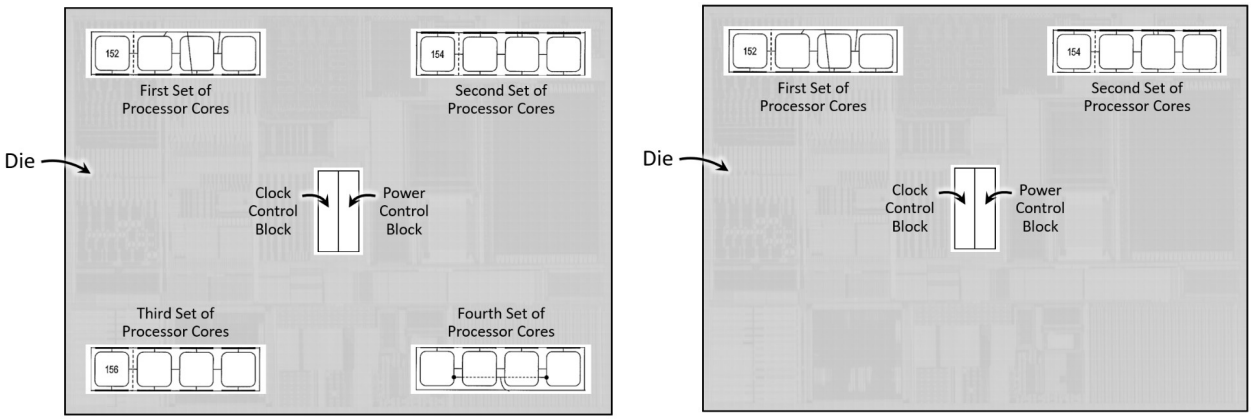
**C. Term #3: "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores"**

| Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction |
|---|---|---|
| #3: "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores"<br><br>U.S. Patent No. 8,549,339, Claim 14<br><br>Proposed by Defendants | "Located in a common region of the first set of processor cores and the second set of processor cores" | Indefinite |

**The Parties' Positions:**

Defendants contend that this term is indefinite because a POSITA would not understand, with reasonable certainty, "both (1) when a component is 'located in a common region,' or not, and (2) when the 'region' is "substantially central to the first set of processor cores and the second set of processor cores,[] or not." Opening at 17.

With respect to the latter, Defendants contend that while "substantially central" is a term of degree, the claims and specification do not provide the necessary guidance as to the scope of the claim term. *Id.* (citing *Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1371 (Fed. Cir. 2014)). Defendants contend that independent Claim 1 and dependent Claim 14 "provide no physical requirement for the individual processor cores of the claimed multi-core processor." *Id.* Defendants contend that a POSITA would understand that "processor cores need not be immediately adjacent in the manner shown in Figure 1[.]" *Id.* Defendants contend that other physical layouts may be possible such as those depicted below.




*Id.* at 18 (citing Opening, Ex. 1 (Villasenor Decl.) at Figure H (left), I (right)). Defendants contend that a POSITA would not know whether the control blocks in Figure H are "substantially central" by virtue of being equidistant from each set of cores, or whether the control blocks are not substantially central given the separation of the processor cores from the control blocks. With respect to Figure I, Defendants contend that "a [POSITA] would not know whether (a) the depicted control blocks are 'substantially central' because they are at the horizontal midpoint between the first and second sets of processor cores, or (b) whether the control blocks are not 'substantially central' because they are not in the same vertical position as the sets of processor cores." *Id.* at 18–19 (citing Opening, Ex. 1 (Villasenor Decl.) at ¶¶ 87, 88).

Defendants contend that the specification does not use the words "central" or the phrase "substantially central." *Id.* at 19. Defendants contend that independent Claim 1 and dependent Claim 14 do not require a physical arrangement of the processor cores, so those claims do not provide any guidance that would help a POSITA understand the scope of this term with reasonable certainty. *Id.*

With respect to the former, Defendants contend that a POSITA would understand sets of processor cores being located in a "common region" means that the "first and second sets of processor cores share a common region where control blocks are located." *Id.* at 19–20 (citing Opening, Ex. 1 (Villasenor Decl.) at ¶ 79). But Defendants contend that the claims do not provide an indication of "what constitutes a "region" corresponding to a set of processor cores or how such regions could be in "common." *Id.* at 20 (citing Opening, Ex. 1 (Villasenor Decl.) at ¶¶ 80–81).

Defendants contend that "common" cannot mean "overlapping" because dependent Claim 9 uses the term "overlapping" and different words are presumed that have different meanings. *Id.* (citing *SimpleAir, Inc. v. Sony Ericsson Mobile Commc'ns AB*, 820 F.3d 419, 431 (Fed. Cir. 2016)).

Defendants contend that specification does not use the words "common region." *Id.* Defendants contend that while the specification uses the words "common area," the specification does not describe sets of processor cores sharing a "common region." *Id.*

In its response, Plaintiff contends that the specification clearly describes both "region" and "common region." Response at 13. Plaintiff contends that the specification uses "region" to refer to sections of the multi-core processor and that "these regions may 'correspond to rows of the two-dimensional array, and the regions may or may not be overlapping.'" *Id.* (citing '339 Patent at 2:20–21, 2:22–23). Based on that, Plaintiff contends that a POSITA would "understand that a

'region' corresponds with the subdivision of the multi-core processor containing the claimed sets of processor cores." *Id.*

With respect to "common region," Plaintiff contends that Claim 14 "refers to the region common to the claimed first and second sets of processor cores and contains the control blocks." *Id.* Plaintiff contends that Defendants attempt to dispute the plain meaning of "common region" by claim differentiation, namely, that Claim 9 recites "overlapping regions" while Claim 14 recites "common region." *Id.* at 13–14. Plaintiff contends that claim differentiation is a rebuttable presumption such that "where neither the plain meaning nor the patent itself commands a difference in scope between two terms, they may be construed identically." *Id.* (quoting *Power Mosfet Techs., L.L.C. v. Siemens AG*, 378 F.3d 1396, 1409–10 (Fed. Cir. 2004)). Plaintiff contends that, in this case, "if, as Defendant[s] argue[], claim 14 has an overlapping meaning with claim 9, that meaning is mandated by the plain meaning and the patent itself and thus the claims should be construed identically, not indefinitely." *Id.* Plaintiff contends that there are other differences between Claims 9 and 14 including that (1) Claim 9 does not require "one or more control blocks" while Claim 14 does and (2) Claim 9 recites two regions, while Claim 14 recites only one. *Id.*

With respect to "substantially central," Plaintiff contends that Defendants "misconstrue[] the grammar of claim 14 to suggest the control blocks are 'substantially central.'" *Id.* Rather, Plaintiff contends that "claim 14 provides that it is the '***common region that is substantially central***' and the 'control blocks [are] located in [the] common region.'" *Id.* at 14–15 (emphasis added, alternations in Plaintiff's brief). Plaintiff contends that the specification describes that the "common region" is the region that is common to the first and second sets of processor. *Id.* at 15.

Plaintiff contends that the specification describes three possibilities for the location of the control blocks: (1) "two different sides of the multicore processor," (2) "the same side of the multi-

core processor," or (3) "in a common area located near the center of the multi-core processor." *Id.* (citing '339 Patent at 2:31–40). Plaintiff contends that Claim 14 is directed towards Option #3. *Id.*

Plaintiff contends that Defendants argue that

> this reading of "common region" as simple a subdivision of the multi-core processor shared by the two sets of processors and "substantially central" as merely within the multi-core processor renders one or the other a superfluity, such superfluity is irrelevant. Even if a subdivision of the multi-core processor within the multi-core processor is redundant, that does not and cannot render the claim indefinite. As explained above, the cannon against superfluity is not absolute, "where neither the plain meaning nor the patent itself commands a difference in scope between two terms, they may be construed identically."

*Id.* at 15–16 (citing *Power Mosfet,* 378 F.3d at 1409–10).

In their reply, with respect to "located in a common region," Defendants contend that Plaintiff "appears to define 'region' as a 'subdivision of the multi-core processor containing the claimed sets of processor cores' based on portions of the specification that focus exclusively on ***processor cores***." *Id.* (citing Response at 13) (emphasis in Defendants' brief). But Defendants contend that the passages Plaintiff cites "do not address how a 'region' or 'common region' should be understood with respect to the processor cores ***and*** control blocks as recited in claim 14." *Id.* (emphasis in Defendants' brief). Defendants contend that even if Plaintiff's understanding is correct, "whether considering 'control blocks' or a 'common region,' the same uncertainty exists regarding when ***either*** is, or is not, "substantially central." *Id.* (emphasis in Defendants' brief).

Defendants contend that Plaintiff

> claims without support that "to be substantially central merely requires [the 'common region'] to be ***within the multi-core processor***", and "the control blocks can be ***anywhere*** within the 'common region'" Taken together, [Plaintiff's] interpretation means that Claim 14 is satisfied when control blocks are within the multi-core processor, full stop. This gross oversimplification substitutes "multi-core processor" for "common region that is substantially central to the first set of processor cores and the second set of processor cores." Thus, rather than providing

> a "standard for measuring the term of degree" "substantially central," [Plaintiff's] attorney argument removes the term from the claim.

*Id.* at 10 (emphases in Defendants' brief, internal citations omitted).

With respect to their claim differentiation argument, Defendants contend that "different terms [("common region" and "overlapping regions")] should be understood to have different meanings," which renders "common region" to be indefinite. *Id.*

In its sur-reply, Plaintiff contends that the specification describes "that a 'region' is merely a subdivision [of] the multi-core processor containing a set of cores" while a "common region" is the subdivision of the multi-core processor containing both sets of cores. Sur-Reply at 8 (citing'339 Patent at 2:20–27). Plaintiff contends that Defendants concede that a "a POSITA understands this phrase means the first and second sets of processor cores share a common region where control blocks are located." *Id.* (citing Opening at 19–20).

With respect to Defendants' claim differentiation argument, Plaintiff contends that "'where neither the plain meaning nor the patent itself commands a difference in scope between two terms, they may be construed identically,' not indefinitely." *Id.* (quoting *Power Mosfet*, 378 F.3d at 1409–10).

Plaintiff contends that the specification provides for the placement of control blocks "in a common area located near the center of the multi-core processor." *Id.* (citing '339 Patent at 2:31–40). Plaintiff further contends that

> Likewise, in the claim itself, because a "region" is a subdivision of the processor containing a set of cores and the "common region" is the region containing both sets, that a "common region" to be "substantially central" to those sets the term becomes a tautology. A group of two things is always substantially central to those things. In effect the claim only requires there to be a common region of the sets of cores and that the control block be placed in it. While the "substantially central" limitation may be superfluous, that is the plain meaning of the term.

*Id.* at 9–10.

**The Court's Analysis:**

After reviewing the parties' arguments and considering the applicable law, the Court agrees with Defendants that the term is indefinite. The Court separately analyzes "common region" and "substantially central."

With respect to the former, the Court agrees that this term is not indefinite. The specification explains that a "region" is a subdivision of the multi-core processor containing the claimed sets of processor cores. '339 Patent at 2:20–23. "Common" is a well-understood English word. Accordingly, the "common region" is the region of that is common to the regions corresponding to the first and second set of processor cores.

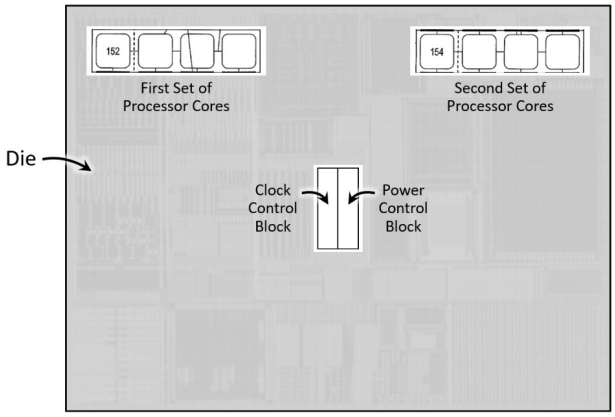
With respect to Defendants' claim differentiation argument, even if "overlapping region" and "common region" have the same meaning, the Court declines to find the latter to be indefinite as claim differentiation alone does not appear to be clear and convincing evidence of indefiniteness. Furthermore, the Court agrees with Plaintiff that there are differences in scope between Claims 9 and 14 other than "overlapping region" and "common region," namely, that (1) Claim 14 requires one or more control blocks while Claim 9 does not and (2) Claim 9 recites two regions, while Claim 14 recites only one. As such, Claims 9 and 14 will have different scopes even if "overlapping region" and "common region" have the same meaning.

Based on the above, the Court concludes that because a POSITA would understand with reasonable certainty the scope of "common region," it is not indefinite. *Nautilus*, 572 U.S. at 910.

On the other hand, the Court concludes that "substantially central" is indefinite for at least the following reasons. ***First***, independent Claim 1 and dependent Claim 14 do not provide any guidance as they do not require a physical arrangement of the processor cores. ***Second***, the specification does not use the words "central" and the phrase "substantially central."

***Third***, Plaintiff contends that the specification describes three possibilities for the location of the control blocks: (1) "two different sides of the multicore processor," (2) "the same side of the multi-core processor," or (3) "in a common area located near the center of the multi-core processor." *Id.* (citing '339 Patent at 2:31–40). But, of these three possibilities, only the third describes applies to this claim term. Even then, because "near the center" in this passage, at best, only paraphrases "substantially central," this passage does not provide the necessary objective boundaries for a POSITA. *Interval Licensing*, 766 F.3d at 1371–72.

***Fourth***, depending on the location of the processor cores, a POSITA may not understand with reasonable certainty whether the control blocks are "substantially central." Using Defendants' Figure H as an example, a POSITA would not know whether the depicted control blocks are "substantially central" as it is unclear whether it requires that the control block to be at the same vertical level as the first and second set of processor cores or whether being in the middle horizontally is sufficient.




Based on the above, the Court concludes that there is clear and convincing evidence that a POSITA would not understand with reasonable certainty the scope of "substantially central." *Nautilus*, 572 U.S. at 910. As such, it is indefinite.

## IV. CONCLUSION

In conclusion, for the reasons described herein, the Court adopts the below constructions as its final constructions.

**SIGNED** this 15th day of October, 2025.

ALAN D ALBRIGHT
UNITED STATES DISTRICT JUDGE

| Term | Plaintiff's Proposed Construction | Defendants' Proposed Construction | Court's Final Construction |
|---|---|---|---|
| #1: "the first clock signal is independent from the second clock signal"<br><br>U.S. Patent No. 8,549,339, Claims 1, 21<br><br>Proposed by Defendants | Plain and ordinary meaning | Plain and ordinary, which requires that the first and second clock signals depend from different reference oscillator clocks | Plain-and-ordinary meaning, wherein the plain and ordinary meaning does not require that the first and second clock signals depend from different reference oscillator clocks. |
| #2: "located in a periphery of the multi-core processor"<br><br>U.S. Patent No. 8,549,339, Claim 5<br><br>Proposed by Defendants | Plain and ordinary meaning | Indefinite | Not indefinite. Plain-and-ordinary meaning. |
| #3: "located in a common region that is substantially central to the first set of processor cores and the second set of processor cores"<br><br>U.S. Patent No. 8,549,339, Claim 14<br><br>Proposed by Defendants | "Located in a common region of the first set of processor cores and the second set of processor cores" | Indefinite | Indefinite |